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Practitioner's Docket No. MI22-1322

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Agarwal, Vishnu K.

Application No.: 09/512,149
Filed: 02/23/00Group No.: 2814
Examiner: M. Pizzaro-Crespo

For: Integrated Circuitry Including a Capacitor With An Amorphous and a Crystalline High K Capacitor Dielectric Region

Commissioner for Patents
Washington, D.C. 20231

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Examiner Interview Summary of February 26, 2004

March 2, 2004
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Total pages 4

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Application Serial No. 09/512,149
Examiner Interview Summary of 02/26/04

MI22-1322

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application Serial No. 09/512,149
Filing Date February 23, 2000
Inventor Vishnu K. Agarwal
Assignee Micron Technology, Inc.
Group Art Unit 2814
Examiner Marcos Pizzaro-Crespo
Attorney's Docket No. MI22-1322
Title: Integrated Circuitry Including A Capacitor With An Amorphous And A Crystalline
High K Capacitor Dielectric Region

EXAMINER INTERVIEW SUMMARY OF FEBRUARY 26, 2004

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Applicant's representative held an interview with Examiner Pizzaro-Crespo on February 26, 2004. Applicant's representative would like to thank Examiner Pizzaro-Crespo for his time and attention to this matter.

Claims 71, 78 and 80 were discussed regarding the various 35 U.S.C.

Application Serial No. 09/512,149
Examiner Interview Summary of 02/26/04

MI22-1322

§112 rejections presented against the respective claims.

Regarding the §112, first paragraph, rejection against claim 71, such claim recites an opening comprises a trench. The Examiner was unable to obtain Applicant's figures during the interview. However, he stated that the originally-filed application does not describe the opening as a trench. During the Examiner Interview of February 26, 2004, the Examiner and Applicant's representative discussed and reviewed the reference, Silicon Processing for the LSI Era, by S. Wolf, vol. 2, pgs. 600-609 which illustrates exemplary openings referred to as trenches. Applicant's representative stated that the openings of Wolf are similarly configured as shown by Fig. 9 of Applicant's originally-filed application, and therefore, at least this Fig. 9 provides written support for a trench. While no agreement was reached, the Examiner stated he would reconsider this rejection once he was able to review Applicant's Figures.

Claim 78 stands rejected under 35 U.S.C. §112, first paragraph, as containing subject matter which was not described in the specification. During an interview with Examiner Pizzaro-Crespo on February 26, 2004, agreement was reached that this is an improper rejection. Claim 78 recites a first electrode layer comprises a monolithic unitary material. However, the Examiner incorrectly referred to claim 78 as reciting a conductive region and addressed this language in his rejection. Applicant's representative pointed out this was a limitation not recited by claim 78, and therefore, the rejection was not relevant. The Examiner

Application Serial No. 09/512,149
Examiner Interview Summary of 02/26/04

MI22-1322

agreed, and therefore, Applicant requests withdrawal of this rejection in the next office action.

Claim 80 stands rejected under the first, second and fourth paragraphs of 35 U.S.C. §112, all based on the same rationale. Claim 80 recites a high K substantially crystalline material layer is less than 80% crystalline. For each rejection, the Examiner alleges that such recitation leaves the percentage range open-ended, that is, lacking a lower limit of the percentage range. During an interview with Examiner Pizzaro-Crespo on February 26, 2004, agreement was reached that this is an improper rejection because independent claim 1 (from which claim 80 depends) provides the lower limit of the percentage range. Claim 1 recites a high K substantially crystalline material layer is at least 70%. The Examiner agreed, and therefore, Applicant requests withdrawal of the three §112 rejections against claim 80 in the next office action.

Respectfully submitted,

Dated: 3-2-04

By: 

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